

CURRICULUM VITAE

Name Trevor Bagnall

Date of birth 23.11.1979

Nationality Australian

Qualification CPEng, RPEQ, B.Eng in Electrical Engineering,
Central Queensland University, Australia

Current role Engineer
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Education

1997 – 2001 Electrical Engineering at Central Queensland University, (AUS)

1998 – 2001 Industrial placement with Queensland Rail Traction Power (AUS)

2000 Industrial placement with ABB Power Electronics, Turgi (CH)

Career

2001 – 2006 Laboratory Engineer – Berner Fachhochschule, Burgdorf (CH): responsible for supporting the mechatronics laboratory's internal and external projects in regard to control systems hardware/circuit board design and software/FPGA design using Matlab/Simulink & VHDL.

2006 – 2009 Control Systems Engineer – ABB Power Electronics, Turgi (CH): responsible for control system design (predominantly in Matlab/Simulink) and commissioning of PCS6000 STATCOMS & SFCs for wind, utility, industrial and rail applications.

2009 – 2010 Sales Engineer – ABB Power Electronics, Turgi (CH): responsible for specifying modifications and upgrades to existing high power rectifiers (thyristor & diode) used in industrial applications (aluminium, copper, smelters, etc..)

2010 – 2011 Senior Freight Projects Engineer – QR National (Aurizon), Brisbane (AUS): responsible for commissioning handover and acceptance of the Siemens E40AC (3700/3800 class) heavy-haul coal locomotive fleet into the Central Queensland network.

2011 – 2019 Principal Engineer – High Voltage Systems, Queensland Rail, Brisbane (AUS): Lead engineer for specifying traction power equipment and configuration of the South East Queensland network. Introduced Static Frequency Converters to 25kV 50Hz AC railways. Conducted harmonic and compatibility studies both rail and utility side, sectioning reviews, protection reviews, earthing reviews, commissioning and acceptance tests. Lead for holistic system modelling (OpenTrack/OpenPowerNet) to inform system dimensioning/integration/options analysis for new projects and evaluate system performance and redundancy for proposed timetables.

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